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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,344	MACY ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,7-14,17-26,29,30,34-36,39-48,52 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7-14,17-26,29,30,34-36,39-48,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, 7-14, 17-26, 29, 30, 34-36, 39-48, 52, and 53 have been examined.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/22/2006 has been entered.

Withdrawn Rejections

3. Applicant, via amendment, has overcome the 35 U.S.C. § 101 rejections set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 7-10, 12-14, 17-19, 21, 23-26, 29, 30, 34, 36, 48, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice et al., U.S. Patent No.

6,816,961, (Herein referred to as Rice) in view of Goodman & Miller, "A Programmer's View of Computer Architecture" (Herein referred to as Goodman).

6. Referring to claims 1, 12, 21, 30, and 36, taking claim 1 as exemplary, Rice has taught a method comprising:

responsive to receiving a single packed shuffle instruction *(byte swap instruction)* designating, with 3 bits, a first register *(first source register; Fig. 7, component 504)* storing a first operand having a set of L data elements *(source field; Fig. 7, component 512)* and designating, with 3 bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each designated with three bits.)*, a second register *(second source register; Fig. 7, component 508)* storing a second operand having a set of L control elements *(condition field; Fig. 7, component 700)*, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L control elements is divided into two portions, the first portion being an operation field occupying the most significant bits of each control element *(The constant loaded into the second operation (having control elements) is shown to have the operation field in the most significant bits; column 8, line 66 – column 9, line 11; Table III)* that indicates an operation to be performed on a resultant element, the second portion being a position selection field *(result field select value)* that is at

least $\log_2 L$ bits wide and indicates a position of one of said L data elements *(column 7, lines 50-56)*

storing a resultant operand in a destination register having L resultant data elements of the same size as the L data elements and the L control elements *(column 7, lines 48-49; Fig. 7)*, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element *(column 7, lines 53-55)*, and is either, the one of the L data elements designated by the position selection field of said control element if said control element's operation field is not set *(i.e. set to zero)*; or zero if said control element's operation field is set to "00001" *(column 7, lines 57-67; Table I)*

Rice does not disclose that the operation field is a flush to zero bit wherein the flush to zero bit alone controls whether a resultant element is flushed to zero and wherein each one of the L control elements is divided into three portions. Rice further does not disclose that the destination register is the first register.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the remove the ability to perform operations on result fields other than the operations indicated by operation fields "00000" and "00001" (i.e. no modification and clearing) since it has been held that eliminating an element and its function is not sufficient to patentably distinguish over the prior art (See *In re Karlson* CCPA 1963). In doing so, the operation field would be specified by a single bit *(a flush to zero bit)* that alone controls whether a resultant element is flushed to zero. As the operation field is specified by a single bit, the remaining four unused bits *(formerly part*

of the five bit operation field) of the each control element would form a third portion of each control element.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

The additional limitation in claim 30 of "and, wherein each of said L masks occupies a particular position in said second operand and is associated with a similarly located data element position in a resultant operand" and a similar limitation in claim 36 is supported at column 6, line 62 – column 7, line 6 and in Fig. 5 of Rice. It is noted that the "masks" of claim 30 and the "shuffle masks" of claim 36 correspond to the "control elements" of claim 1

7. Referring to claims 4, 14, and 25, taking claim 4 as exemplary, Rice and Goodman have taught the method of claim 1 wherein said control element *(condition field)* is to designate a first operand data element *(source filed)* by a data element position number *(result field select value) (Rice; column 7, lines 49-55)*.

8. Referring to claim 7, Rice and Goodman have taught the method of claim 1 further comprising outputting a resultant data block comprising data that was shuffled

from said first operand in response to said control elements of said second operand *(Rice; column 7, lines 32-42)*.

9. Referring to claims 8 and 26, taking claim 8 as exemplary, Rice and Goodman have taught the method of claim 1 wherein each of said data elements comprises a byte of data *(Rice; column 6, line 62 – column 7, line 5; See Fig. 7, component 512)*.

10. Referring to claims 9 and 18, taking claim 9 as exemplary, Rice and Goodman have taught the method of claim 8 wherein each of said control elements is a byte wide *(Rice; column 6, line 62 – column 7, line 5; See Fig. 7, component 700)*.

11. Referring to claims 10 and 19, taking claim 10 as exemplary, Rice and Goodman have taught the method of claim 9 wherein L is 8 and wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data *(Rice; column 6, lines 19-23; See Fig. 7, components 504, 508, and 524)*.

12. Referring to claim 13, Rice and Goodman have taught the apparatus of claim 12 wherein each of said L control elements occupies a position in said second operand and is associated with a similarly located data element position in a resultant *(Rice; See Fig. 5; column 6, line 62 – column 7, line 6)*.

13. Referring to claims 17 and 23, taking claim 17 as exemplary, Rice and Goodman have taught the apparatus of claim 12 wherein said shuffle instruction is to further cause said execution unit to generate a resultant having L data element positions that have been filled based on said set of L control elements *(Rice; column 7, lines 32-42)*.

14. Referring to claim 24, Rice and Goodman have taught the article of manufacture comprising the machine readable storage medium of claim 23 wherein each of said L

control elements is associated with a similarly located data element position in a resultant *(Rice; column 6, line 62 – column 7, line 6)*.

15. Referring to claim 29, Rice and Goodman have taught the article of manufacture of claim 21 wherein said data stored by said machine readable storage medium *(Rice; memory; column 3, lines 1-26)* represents a computer instruction, which, if executed by a machine, causes said machine to perform said predetermined function *(Rice; column 6, lines 25-53)*.

16. Referring to claim 34, Rice and Goodman have taught the method of claim 30 wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data (column 6, lines 19-23; See Fig. 7, components 504, 508, and 524).

17. Referring to claim 48, Rice has taught a system comprising:

a memory to store data and instructions *(memory; Fig. 1, component 14)*;

a processor *(processing core; Fig. 1, component 12)* coupled to said memory on a bus *(See Fig. 1)*, said processor operable to perform a shuffle operation *(byte swap instruction; column 6, lines 25-54)*, said processor comprising:

a bus unit *(See Fig. 1)* to receive a single packed shuffle instruction, from said memory, said instruction to designate, with 3 bits, a first register *(first source register; Fig. 5, component 504)* storing L data elements *(source fields; Fig. 5, component 512)* from a first operand, and to designate, with three bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each*

designated with three bits.), L shuffle control elements *(condition fields; Fig. 7, component 700)* from a second operand *(second source register; Fig. 7, component 508)*, wherein the first operand and second operand are of same size and each of the L data elements and L control elements are of a same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L control elements is divided into two portions, the first portion being an operation field occupying the most significant bits of each control element *(The constant loaded into the second operation (having control elements) is shown to have the operation field in the most significant bits; column 8, line 66 – column 9, line 11; Table III)* that indicates an operation to be performed on a resultant element, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements *(column 7, lines 50-56)*

an execution unit *(processing path; Fig. 2, component 56)* coupled to said bus unit, said execution unit to execute said single packed shuffle instruction *(column 4, lines 46-61)*, said single packed shuffle instruction to cause said execution unit to:

store a resultant operand in a destination register having L resultant data elements of the same size as the L data elements and the L control elements *(column 7, lines 48-49; Fig. 7)*, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same

position as the resultant data element *(column 7, lines 53-55)*, and is either, the one of the L data elements designated by the position selection field of said control element if said control element's operation field is not set *(i.e. set to zero)*; or zero if said control element's operation field is set to "00001" *(column 7, lines 57-67; Table I)*

Rice does not disclose that the operation field is a flush to zero bit wherein the flush to zero bit alone controls whether a resultant element is flushed to zero and wherein each one of the L control elements is divided into three portions. Rice further does not disclose that the destination register is the first register.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the remove the ability to perform operations on result fields other than the operations indicated by operation fields "00000" and "00001" (i.e. no modification and clearing) since it has been held that eliminating an element and its function is not sufficient to patentably distinguish over the prior art (See *In re Karlson* CCPA 1963). In doing so, the operation field would be specified by a single bit *(a flush to zero bit)* that alone controls whether a resultant element is flushed to zero. As the operation field is specified by a single bit, the remaining four unused bits *(formerly part of the five bit operation field)* of the each control element would form a third portion of each control element.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

18. Referring to claim 52, Rice and Goodman have taught the system of claim 48 wherein each data element *(source fields; Fig. 7, component 512)* is a byte wide, each shuffle command element *(condition fields; Fig. 7, component 700)* is a byte wide, and L is 8 *(See Fig. 7)*.

19. Referring to claim 53, Rice and Goodman have taught the system of claim 48 wherein said first operand *(first source register; Fig. 7, component 504)* is 64 bits long and said second operand *(second source register; Fig. 7, component 508)* is 64 bits long (See Fig. 7).

20. Claims 11, 20, 22, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice in view of Goodman and, further, in view of the examiner's taking of Official Notice.

21. Referring to claims 11, 20, and 35, taking claim 11 as exemplary, Rice and Goodman have taught the method of claim 9 wherein L is 8 and wherein said first

operand, said second operand, and said resultant are each comprised of 64-bit wide packed data *(column 6, lines 1-23)*.

Rice has not explicitly taught that L is 16 and wherein the first operand, second operand, and said resultant are each comprised of 128-bit wide packed data.

However, the examiner takes Official Notice that 128-bit wide packed data operands are conventional and well known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the packed data operands of Rice to be 128-bit wide instead of 64-bit wide (thereby making L equal 16) since doing so would allow an operation to be performed upon more byte sized elements at a time than a 64-bit wide packed data operand.

22. Referring to claim 22, Rice and Goodman have taught the article of manufacture of claim 21.

Rice has not explicitly taught that said data stored by said machine readable storage medium represents an integrated circuit design, which when fabricated performs said predetermined function in response to a single instruction.

However, the Office take Official Notice that a Hardware Description Language (HDL) data representation of an integrated circuit design, stored by a machine readable storage medium, that when fabricated performs a predetermined function in response to single instruction is conventional and well known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the data stored on a machine readable storage medium

of Rice to be a Hardware Description Language data representation of an integrated circuit design on a machine readable medium that when fabricated performs a predetermined function in response to a single instruction since doing so would provide storage for an integrated circuit design.

23. Claims 39-43, 45, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice in view of Goodman and, further, in view of Hoyle et al., U.S. Patent Application Publication 2005/0188182 (Herein referred to as Hoyle).

24. Referring to claim 39, Rice has taught an apparatus comprising:

a first memory location *(first source register; Fig. 5, component 504)* to store a plurality of source data elements *(source fields; Fig. 5, component 512)*;

a second memory location *(second source register; Fig. 7, component 508)* to store a plurality of control elements *(condition fields; Fig. 7, component 700)*, each of said control elements to correspond to a resultant data element position *(result field; Fig. 7, component 528) (column 6, line 62 – column 7, line 2; See Fig. 7)*, and

wherein each one of the L control elements is divided into two portions, the first portion being an operation field occupying the most significant bits of each control element *(The constant loaded into the second operation (having control elements) is shown to have the operation field in the most significant bits; column 8, line 66 – column 9, line 11; Table III)* that indicates an operation to be performed on a resultant element,

the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements *(column 7, lines 50-56)*

control logic *(logic wires from second source register; See Fig. 7)* coupled to said first memory location and said second memory location *(second source register)*, said control logic in response to the receipt of a single packed shuffle instruction designating, with three bits *(The first and second memory locations are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second memory locations are each designated with three bits.)*, a first memory location storing a first operand having a set of L data elements and designating a second memory location storing a second operand having a set of L control elements, wherein the first operand and the second operand are of a same size and each of the L data elements and L control elements are of a same size, to generate a plurality of selection signals and a plurality of operation signals, an operation signal generated when a control element's operation field is set *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*;

a first plurality of multiplexers *(multiplexers; Fig. 7)* coupled to said first memory location *(second source register)* and said plurality of selection signals (*logic wires from second source register)*, each of said first plurality of multiplexers to store a resultant operand in a destination memory location having L resultant data elements of the same size as the L data elements and the L control elements, wherein the value of each resultant data element is controlled by the position selection signal of the L control

elements in the same position as the resultant data element *(column 7, lines 43-56)*, and is the one of the L data elements *(source fields)* for a specific resultant data element position *(result field)* in response to a selection signal corresponding to said specific resultant data element position *(column 7, lines 2-10, 33-49)*; and

a processing component *(operand processor; Fig. 7, component 704)* coupled to said first plurality of multiplexers and to said plurality of operation signals, each of said processing components associated with a specific resultant data element position *(result field)*, each of said processing components to output a zero if its operation signal indicates an operation field of "00001" or to output a data element shuffled for that specific resultant data element position *(column 7, lines 43-67; Table I)*.

Rice does not disclose that the operation field is a flush to zero bit wherein the flush to zero bit alone controls whether a resultant element is flushed to zero and wherein each one of the L control elements is divided into three portions. Rice further does not disclose that the destination register is the first register.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the remove the ability to perform operations on result fields other than the operations indicated by operation fields "00000" and "00001" (i.e. no modification and clearing) since it has been held that eliminating an element and its function is not sufficient to patentably distinguish over the prior art (See *In re Karlson* CCPA 1963). In doing so, the operation field would be specified by a single bit *(a flush to zero bit)* that alone controls whether a resultant element is flushed to zero. As the operation field is specified by a single bit, the remaining four unused bits *(formerly part*

of the five bit operation field) of the each control element would form a third portion of each control element.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the apparatus of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

Rice has not explicitly taught that the processing components are multiplexers.

Hoyle also taught a system for intermingling/swapping bytes that uses a plurality of multiplexers to select between zero and a shuffled data element *(See Fig. 7c, paragraphs 94-96, 119)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to replace the processing component *(operand processor)* of Rice with the multiplexer of Hoyle.

The suggestion/motivation for doing so would have been that selection between zero and a shuffled data element would be simplified as would have been recognized by one of ordinary skill in the art.

25. Referring to claim 40, Rice, Goodman, and Hoyle have taught the apparatus of claim 39 wherein said plurality of source data elements *(source fields)* is a first packed data operand *(Rice; column 6, lines 38-41; column 6, line 62 – column 7, line 5)*.

26. Referring to claim 41, Rice, Goodman, and Hoyle have taught the apparatus of claim 40 where said plurality of control elements *(condition fields)* is a second packed data operand *(Rice; column 6, lines 38-41; column 6, line 62 – column 7, line 5)*.

27. Referring to claim 42, Rice, Goodman, and Hoyle have taught the apparatus of claim 40 wherein said first and second memory locations are a single instruction multiple data registers *(Rice; column 5, lines 58-67)*.

28. Referring to claim 43, Rice, Goodman, and Hoyle have taught the apparatus of claim 42 wherein:

said first packed operand is 64 bits long and each of said source data elements is a byte wide *(Rice; column 6, lines 19-22; column 6, line 62 – column 7, line 5)*; and

said second packed operand is 64 bits long and each of said control elements is a byte wide *(Rice; column 6, lines 19-22; column 6, line 62 – column 7, line 5)*.

29. Referring to claim 45, Rice has taught an apparatus comprising:

control logic *(logic wires from second source register; See Fig. 7)* to receive a single packed shuffle instruction designating, with three bits, a first memory location *(first source register; Fig. 7, component 504)* storing a first operand having a set of M data elements *(source fields; Fig. 7, component 512)* and designating, with three bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each designated with three bits.)*, a second memory location *(second source register; Fig. 7, component 508)* storing a second operand having a set of L shuffle masks *(condition fields; Fig. 7, component 700)*, wherein each of the M data elements and L shuffle masks are of a

same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L shuffle masks is divided into two portions, the first portion being an operation field occupying the most significant bits of each control element *(The constant loaded into the second operation (having control elements) is shown to have the operation field in the most significant bits; column 8, line 66 – column 9, line 11; Table III)* that indicates an operation to be performed on a resultant element, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements *(column 7, lines 50-56)*; and

wherein each shuffle mask is associated with a unique resultant data element position *(result field; Fig. 7, component 528)* controlled by the position selection field of said shuffle mask, said control logic to provide a select signal *(result field select value output)* and an operation signal *(operation field output)* for each resultant data element position; and *(column 7, lines 2-10, 50-67; See Fig. 7)*

a set of L processing components *(operand processors)* coupled to said control logic, wherein each processing component is also associated with a unique resultant data element position *(result field)*, each processing component to output to a destination memory location either, a zero if said shuffle mask's operation signal operation signal indicates an operation field of "00001" or the one of the M data elements designated by the select signal of said shuffle mask if said shuffle mask's

operation signal is inactive *(i.e. indicates an operation field of "00000") (column 7, lines 43-67; Table I).*

Rice does not disclose that the operation field is a flush to zero bit wherein the flush to zero bit alone controls whether a resultant element is flushed to zero and wherein each one of the L control elements is divided into three portions. Rice further does not disclose that the destination register is the first register.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the remove the ability to perform operations on result fields other than the operations indicated by operation fields "00000" and "00001" (i.e. no modification and clearing) since it has been held that eliminating an element and its function is not sufficient to patentably distinguish over the prior art (See *In re Karlson* CCPA 1963). In doing so, the operation field would be specified by a single bit *(a flush to zero bit)* that alone controls whether a resultant element is flushed to zero. As the operation field is specified by a single bit, the remaining four unused bits *(formerly part of the five bit operation field)* of the each control element would form a third portion of each control element.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199).*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the apparatus of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

Rice has not explicitly taught that the processing components are multiplexers.

Hoyle also taught a system for intermingling/swapping bytes that uses a plurality of multiplexers to select between zero and a shuffled data element *(See Fig. 7c, paragraphs 94-96, 119)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to replace the processing component *(operand processor)* of Rice with the multiplexer of Hoyle.

The suggestion/motivation for doing so would have been that selection between zero and a shuffled data element would be simplified as would have been recognized by one of ordinary skill in the art.

30. Referring to claim 46, Rice, Goodman, and Hoyle have taught the apparatus of claim 45 further comprising a register *(destination register; Fig. 7, component 524)* with L unique data element positions *(result field; Fig. 7, component 528)*, each data element position to hold an output from its associated multiplexer *(column 7, lines 33-49; See Fig. 7)*.

31. Claims 44 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice in view of Goodman in view of Hoyle and, further, in view of the examiner's taking of Official Notice.

32. Referring to claims 44 and 47, taking claim 44 as exemplary, Rice, Goodman, and Hoyle have taught the apparatus of claim 42, wherein:

said first packed operand is 64 bits long and each of said source data elements is a byte wide *(Rice; column 6, lines 1-23)*; and

said second packed operand is 64 bits long and each of said control elements in a byte wide *(Rice; column 6, lines 1-23)*.

Rice has not explicitly taught that the first and second packed operands are 128 bits long.

However, the examiner takes Official Notice that 128 bit long packed operands are conventional and well known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the packed operands of Rice to be 128-bit wide instead of 64-bit wide since doing so would allow an operation to be performed upon more byte sized elements at a time than a 64-bit wide packed operand.

Conclusion

33. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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